

Fig. 1 is a block diagram of a pixel circuit 2400. The pixel circuit 2400 includes a gate signal driver circuit 2412, a source signal driver circuit 2413, and a pixel portion 2414. The gate signal driver circuit 2412 is connected to the source signal driver circuit 2413 and the pixel portion 2414. The source signal driver circuit 2413 is connected to the pixel portion 2414. The pixel portion 2414 is connected to the gate signal driver circuit 2412 and the source signal driver circuit 2413. The pixel circuit 2400 is connected to a data bus 2405 and a gate bus 2404. The data bus 2405 is connected to the pixel circuit 2400 and the gate bus 2404. The gate bus 2404 is connected to the pixel circuit 2400 and the data bus 2405. The pixel circuit 2400 is connected to a source bus 2403 and a gate bus 2402. The source bus 2403 is connected to the pixel circuit 2400 and the gate bus 2402. The gate bus 2402 is connected to the pixel circuit 2400 and the source bus 2403. The pixel circuit 2400 is connected to a source bus 2401 and a gate bus 2400. The source bus 2401 is connected to the pixel circuit 2400 and the gate bus 2400. The gate bus 2400 is connected to the pixel circuit 2400 and the source bus 2401.

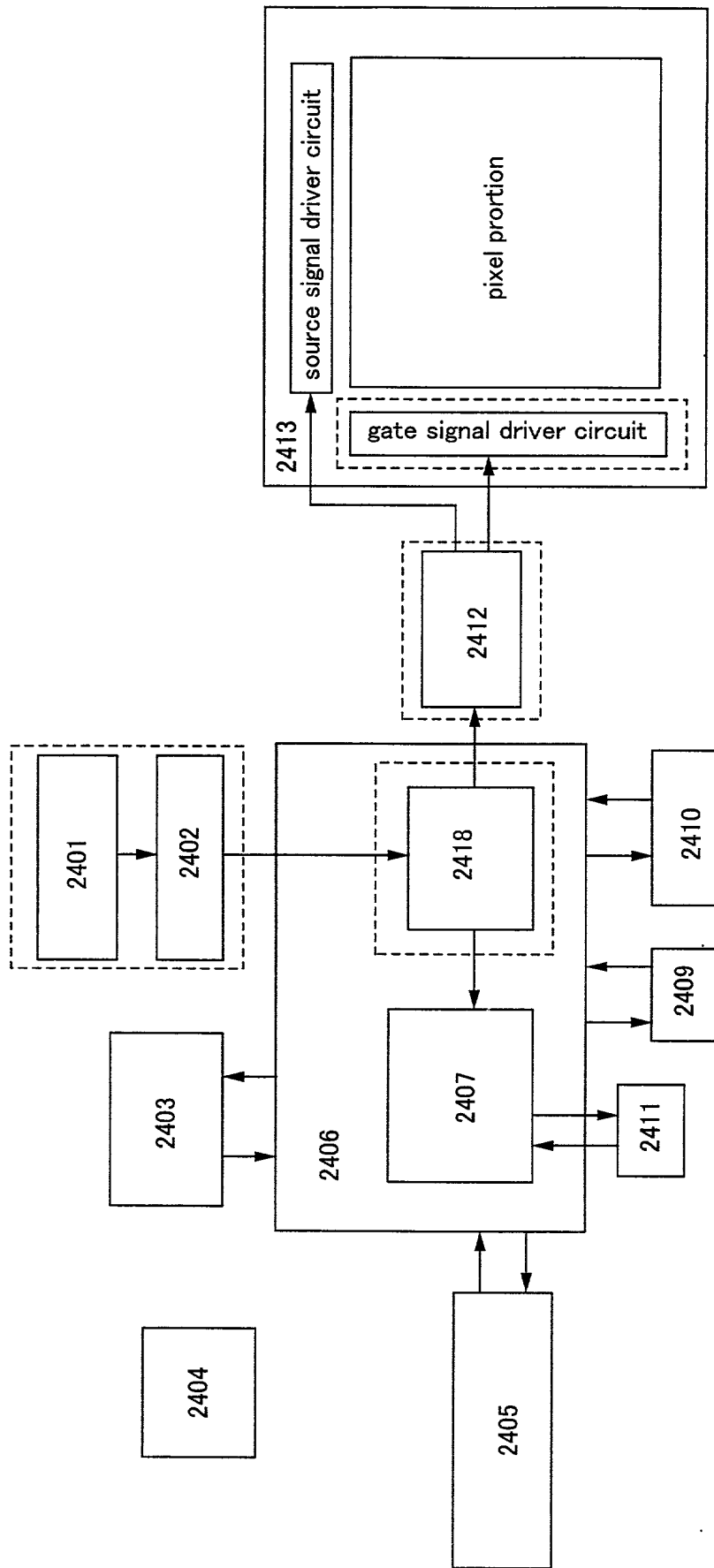


Fig. 1

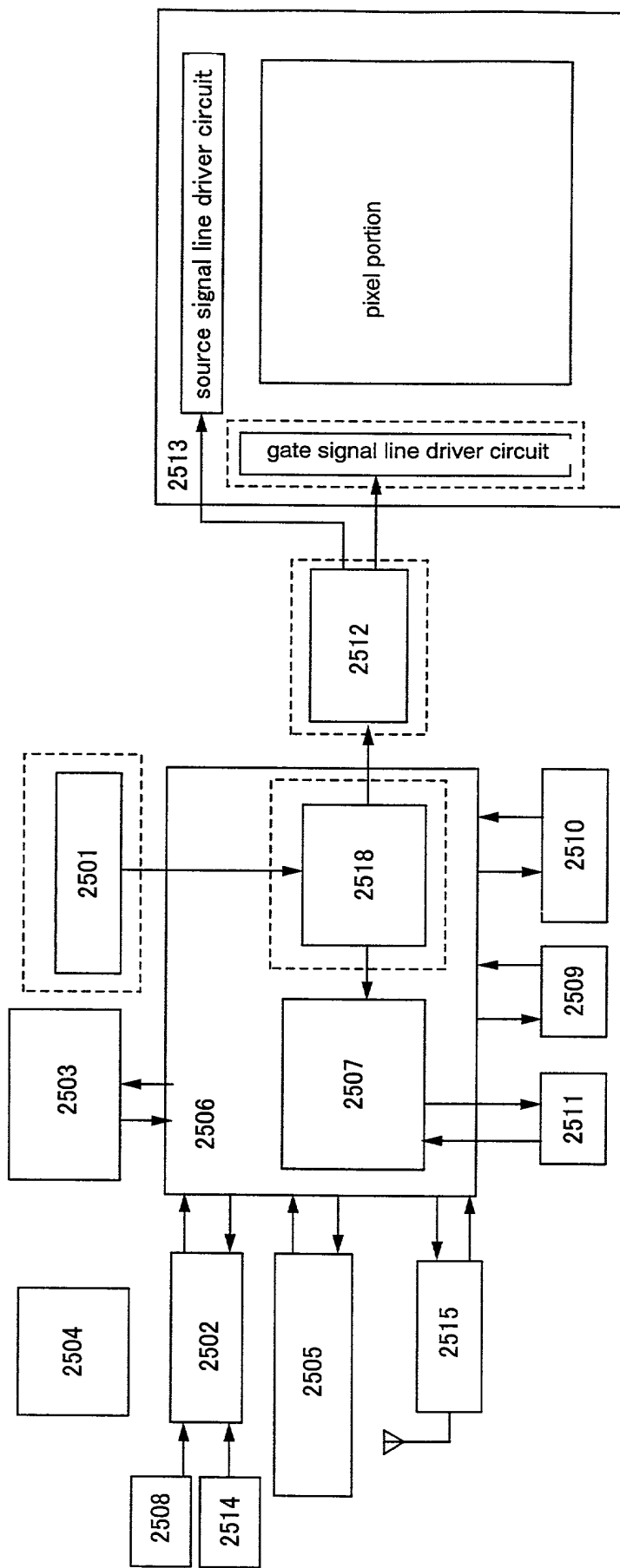


Fig. 2

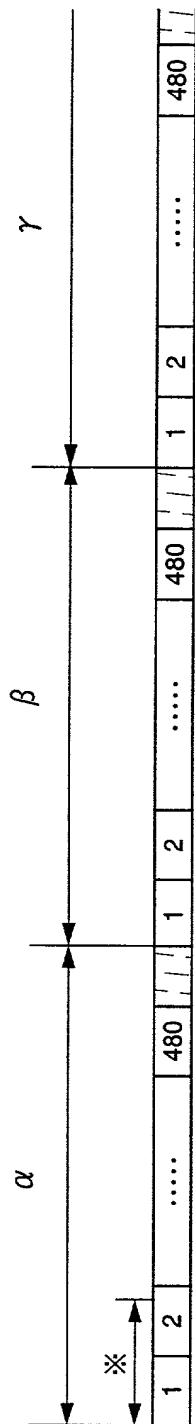


Fig. 3A

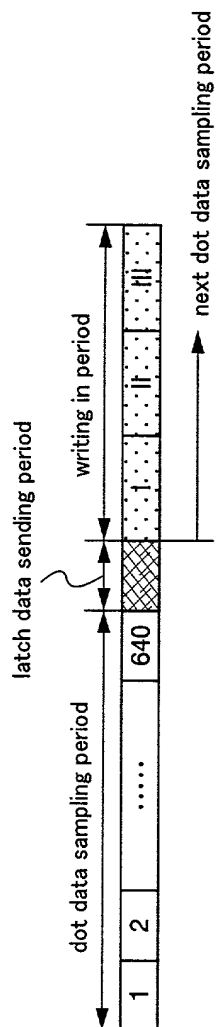


Fig. 3B

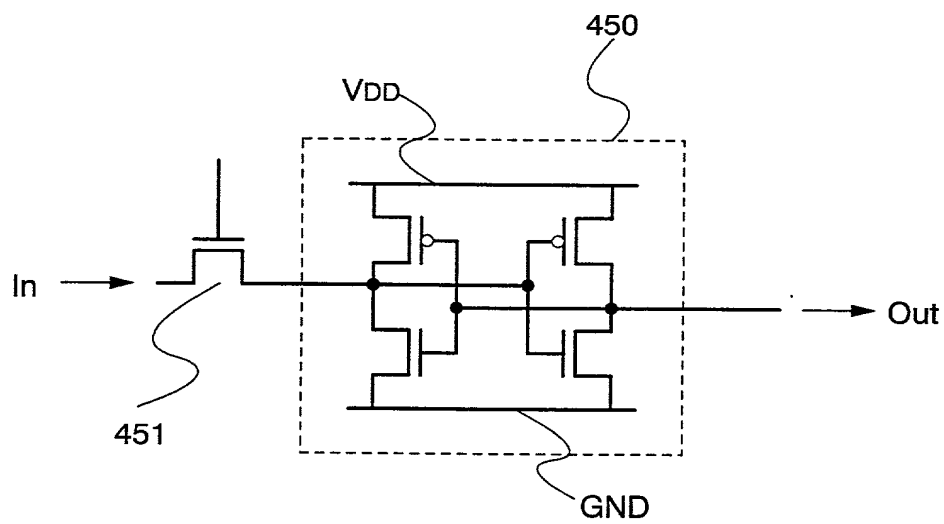


Fig. 4

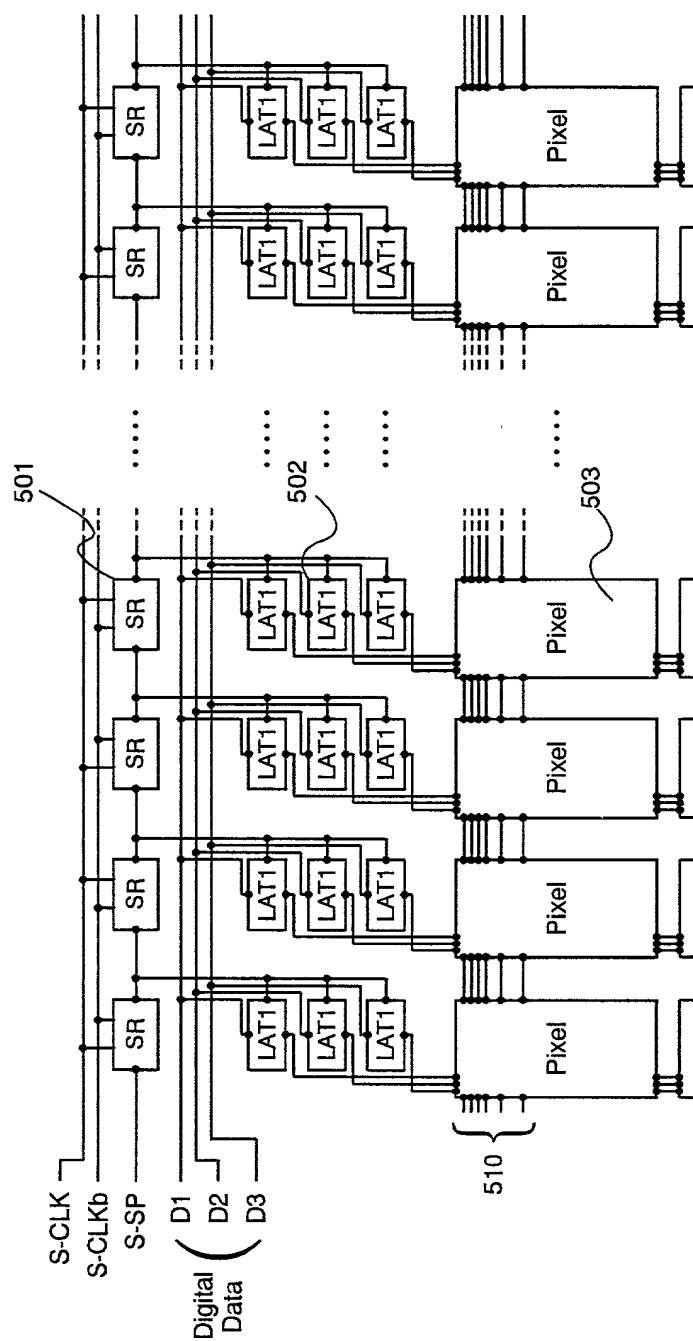


Fig. 5

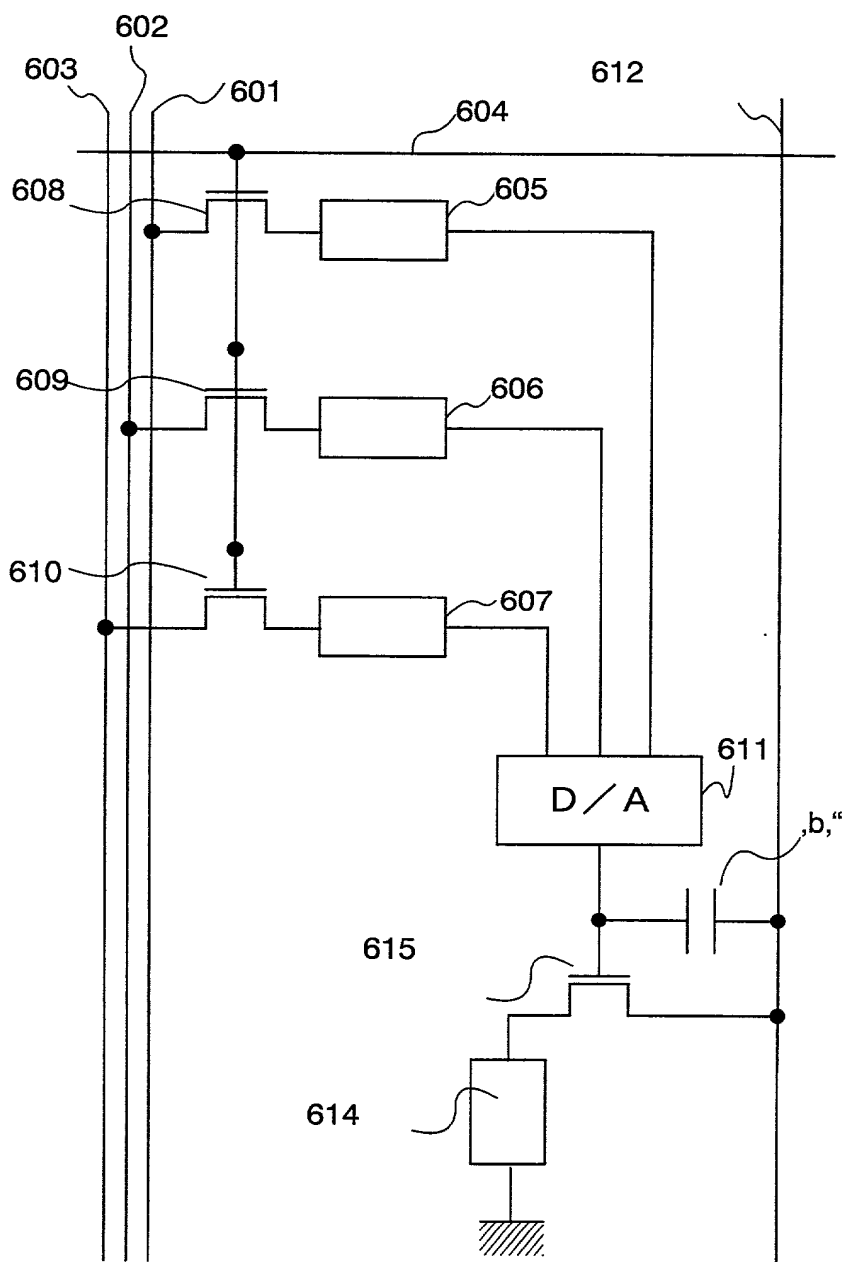


Fig. 6

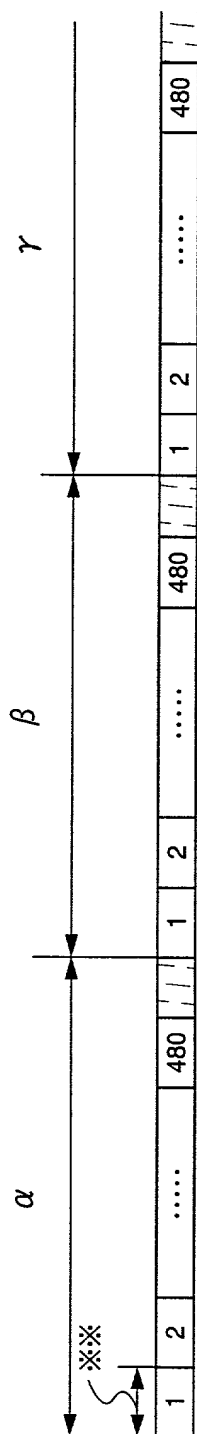


Fig. 7A

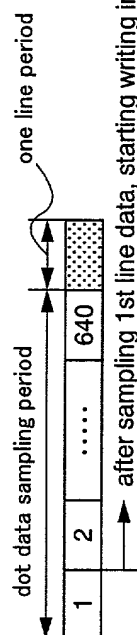


Fig. 7B

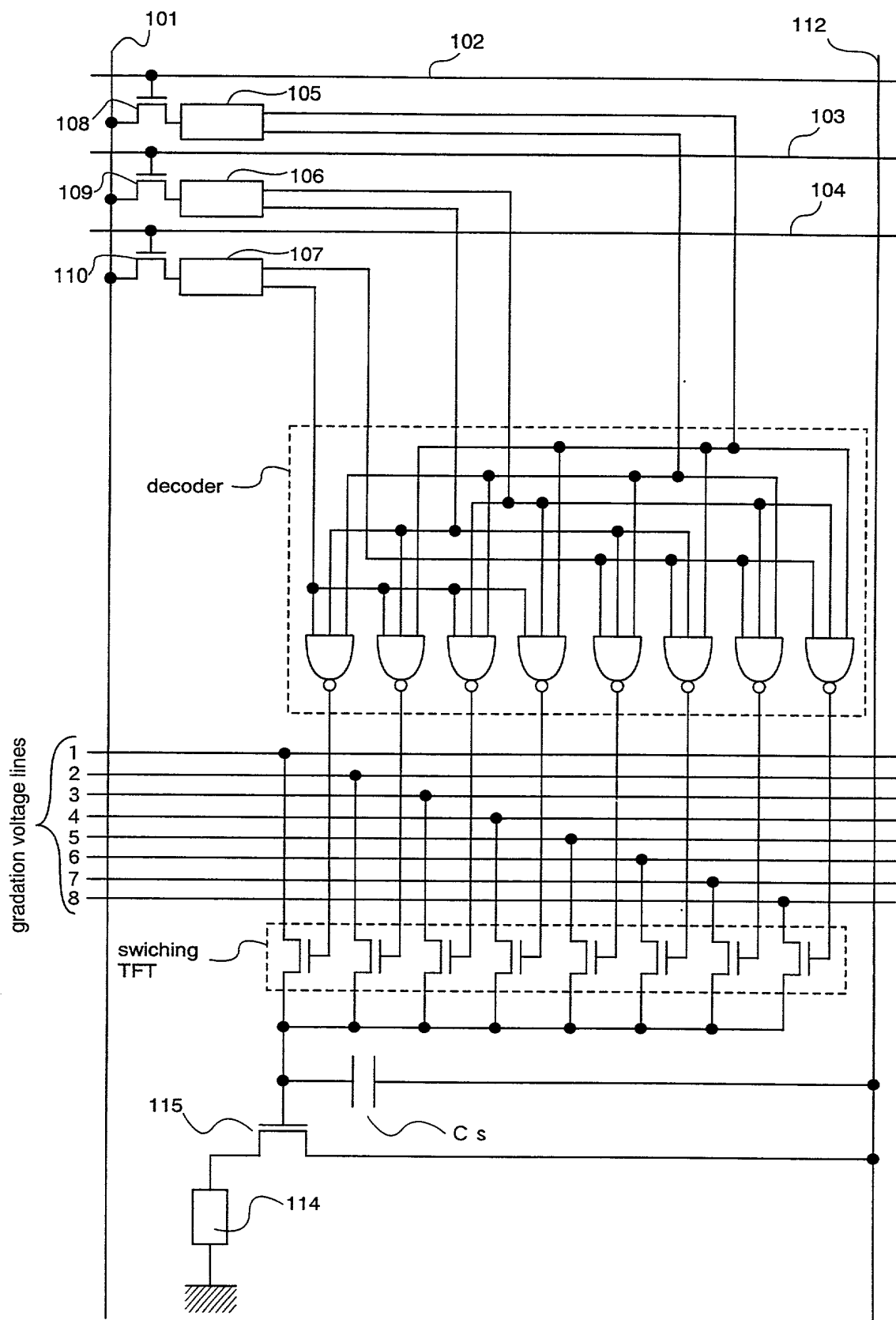


Fig. 8

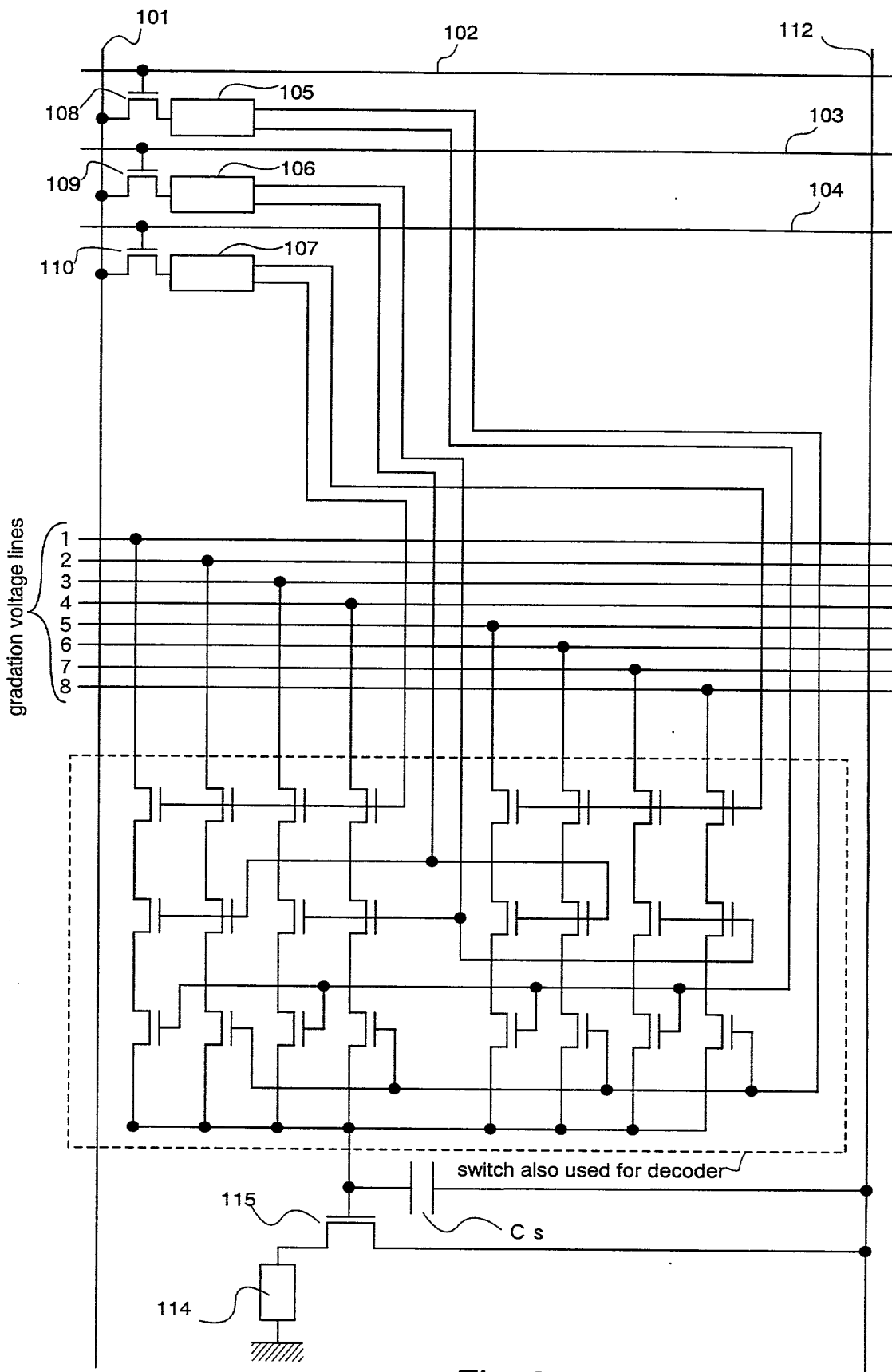


Fig. 9

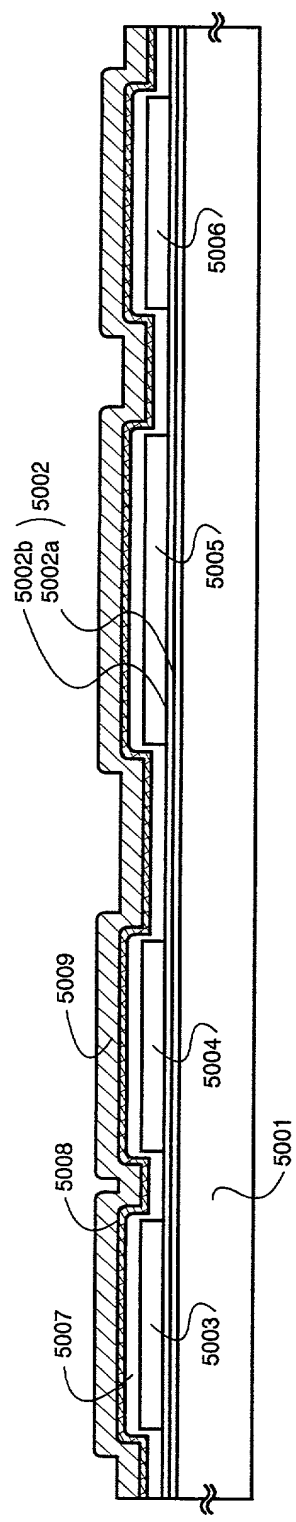


Fig. 10A

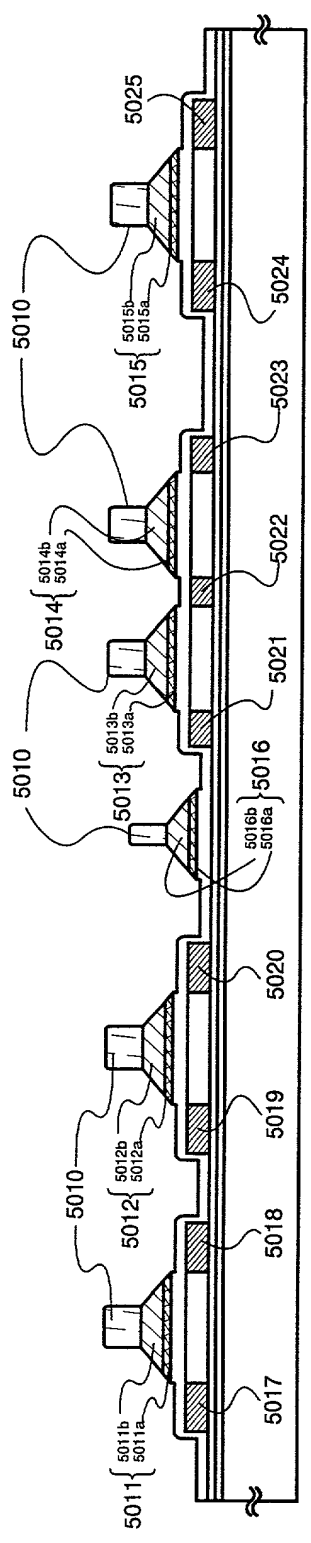


Fig. 10B

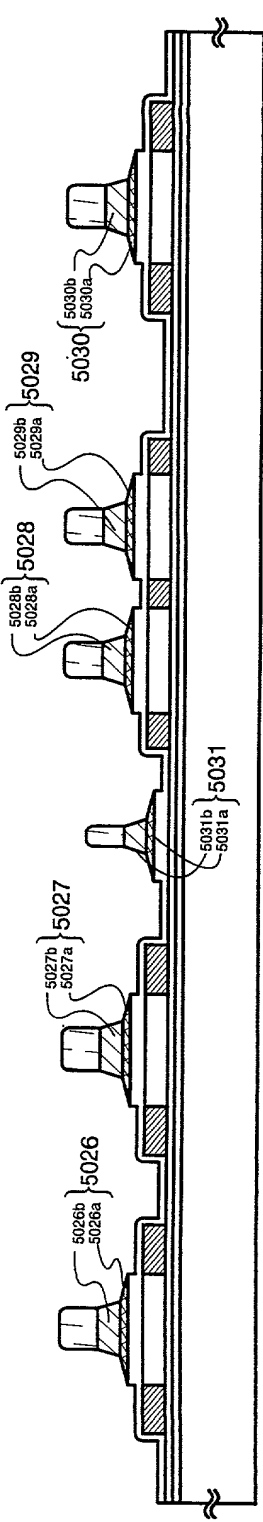


Fig. 10C

FIG. 11A is a cross-sectional view of a portion of a semiconductor device. The device includes a substrate 5032, a gate stack 5033, a gate stack 5034, a gate stack 5035, and a gate stack 5036. The gate stacks are formed on the substrate and are separated by spacers. The spacers are formed on the substrate and are separated by the gate stacks. The gate stacks are formed on the substrate and are separated by the spacers. The spacers are formed on the substrate and are separated by the gate stacks.

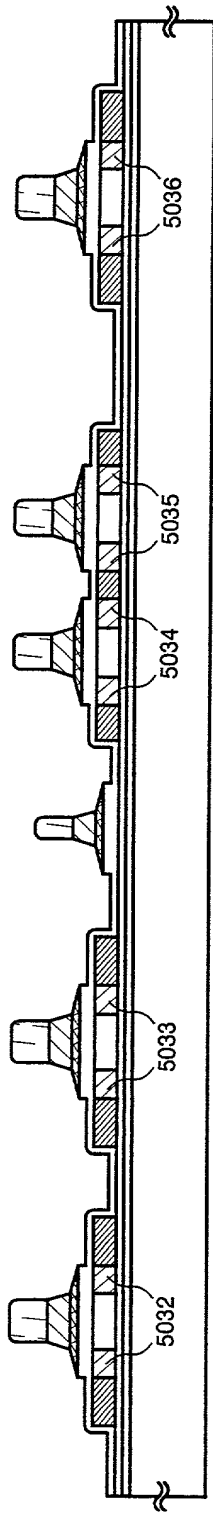


Fig. 11A

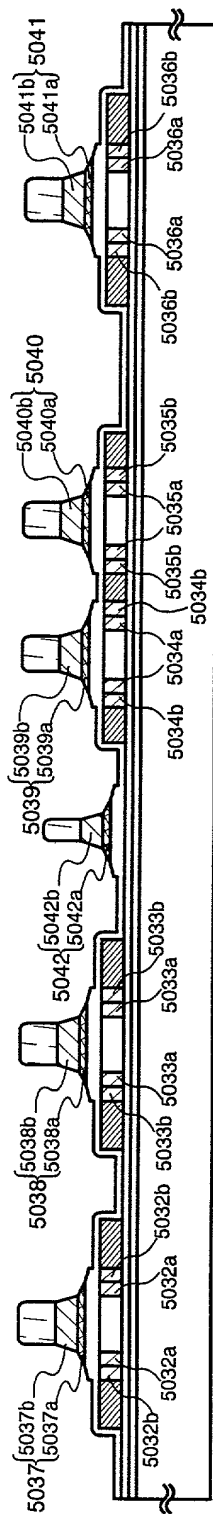


Fig. 11B

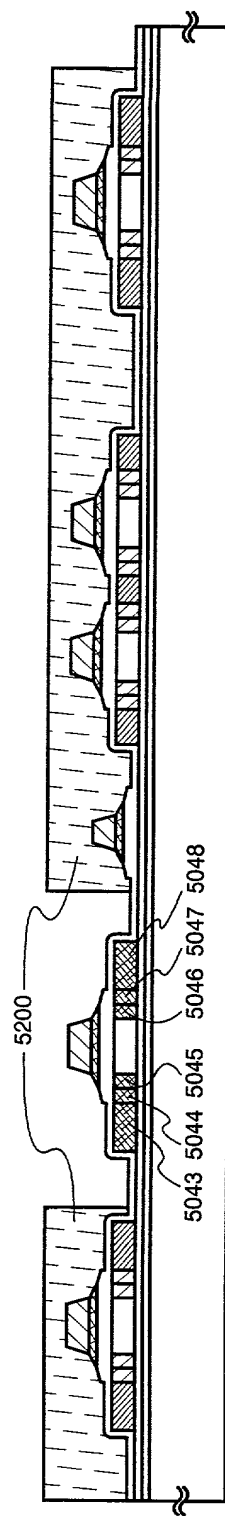


Fig. 11C

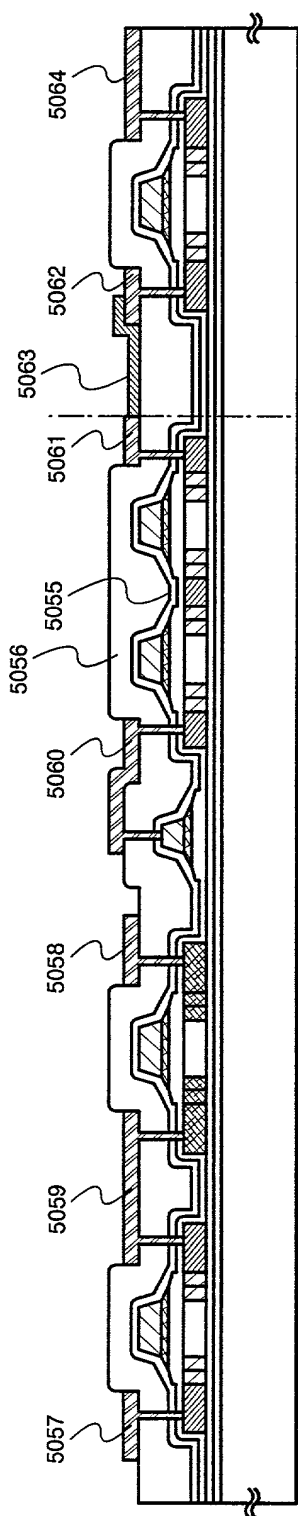


Fig. 12A

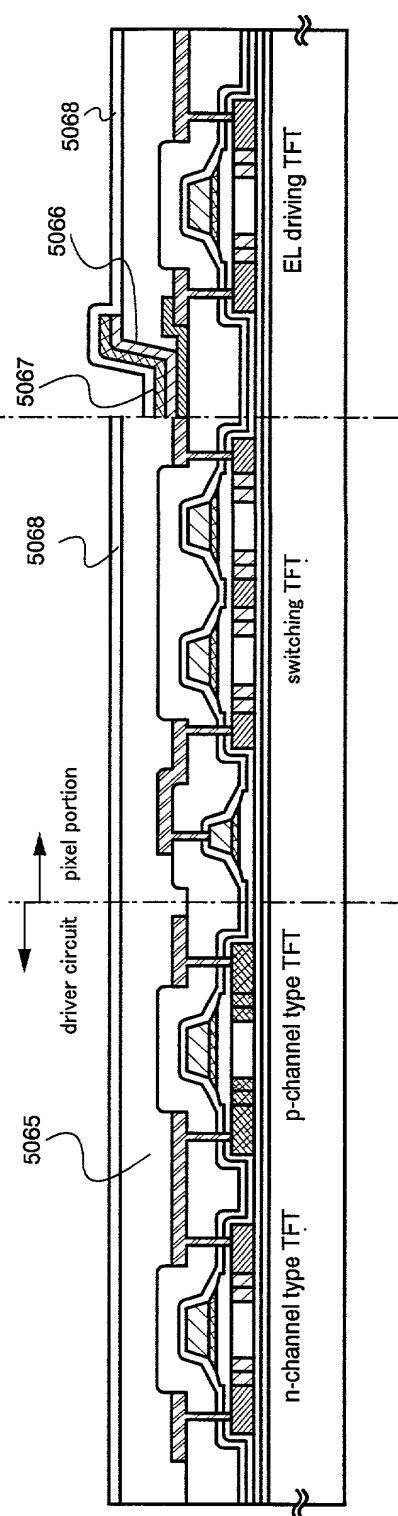


Fig. 12B

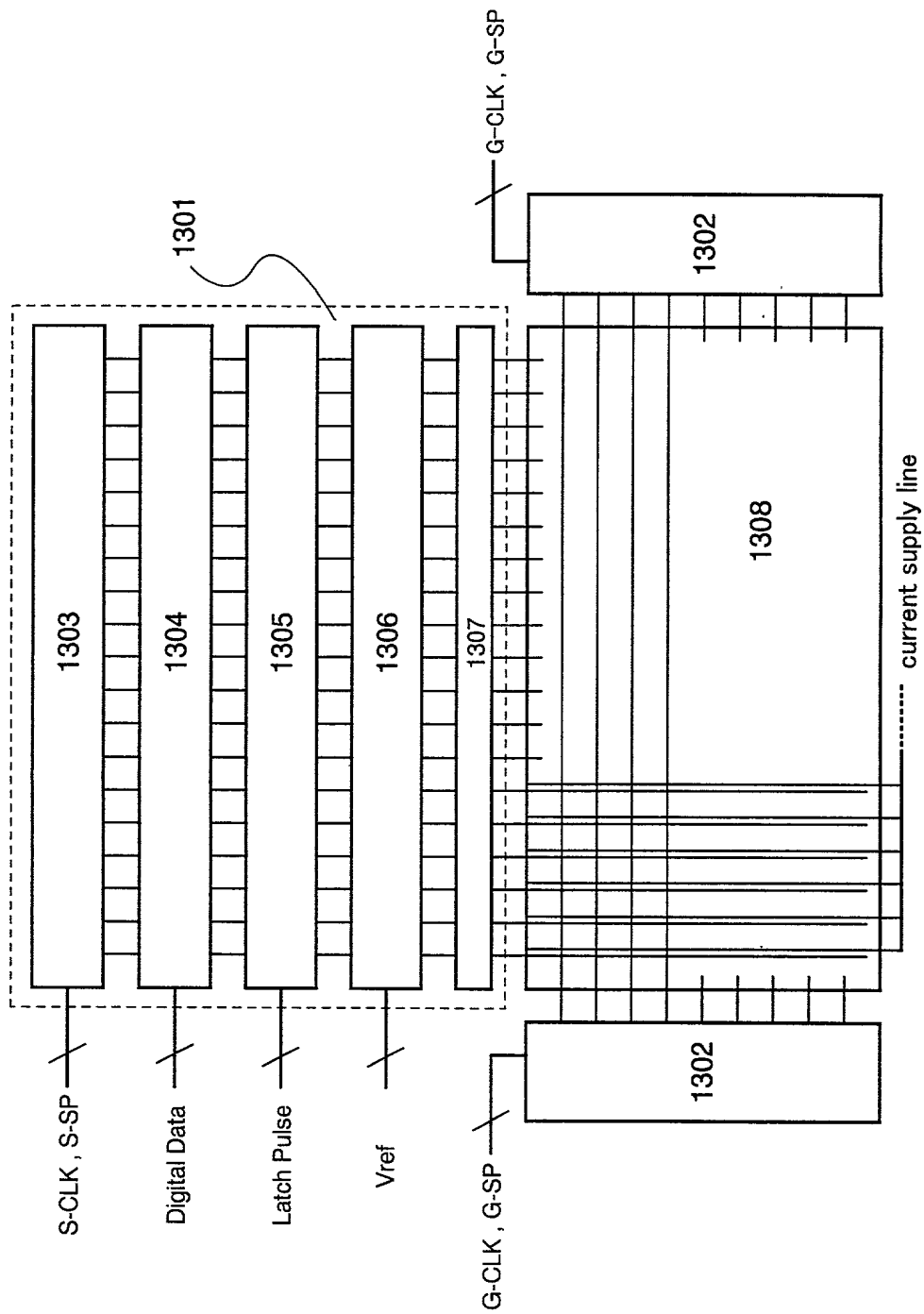


Fig. 13

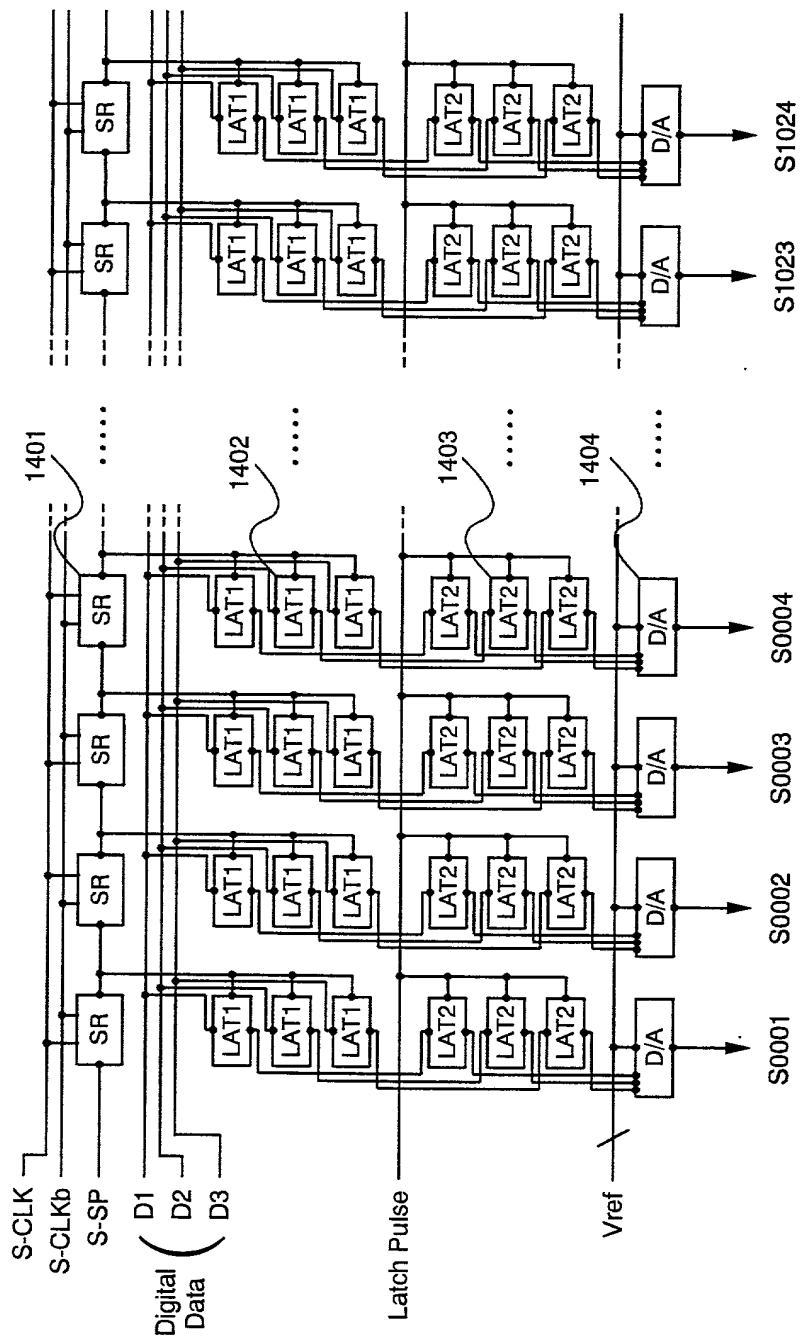


Fig. 14

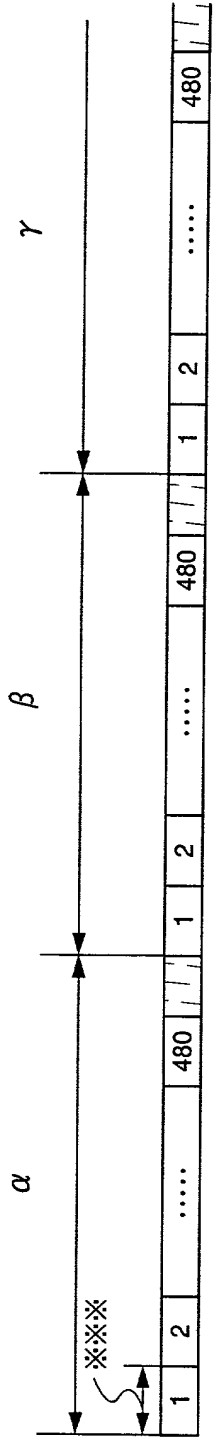


Fig. 18A

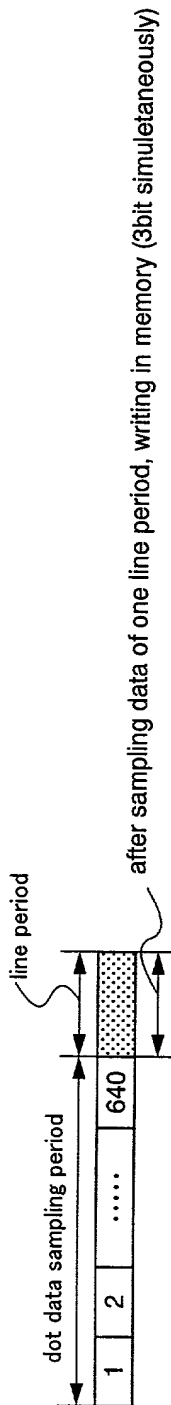


Fig. 18B

Fig. 19A

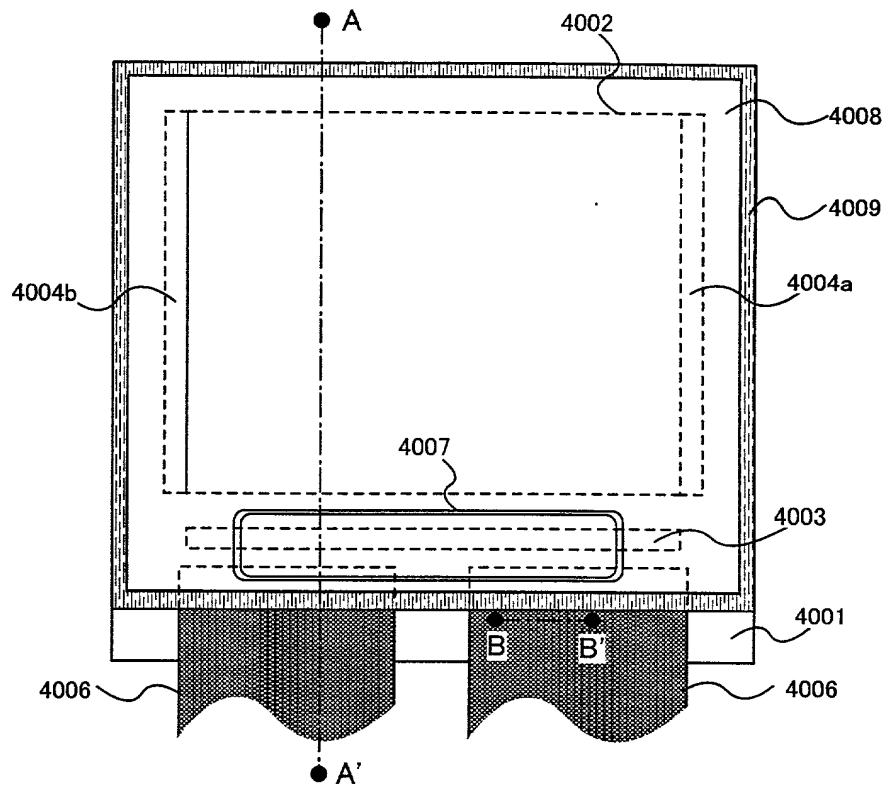


Fig. 19B

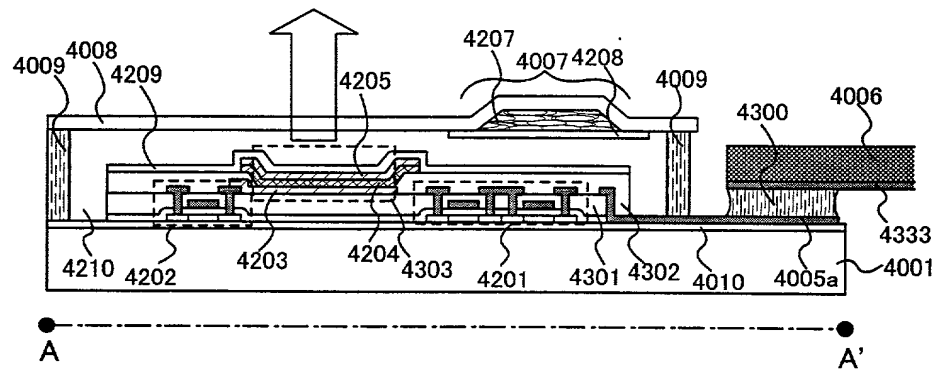
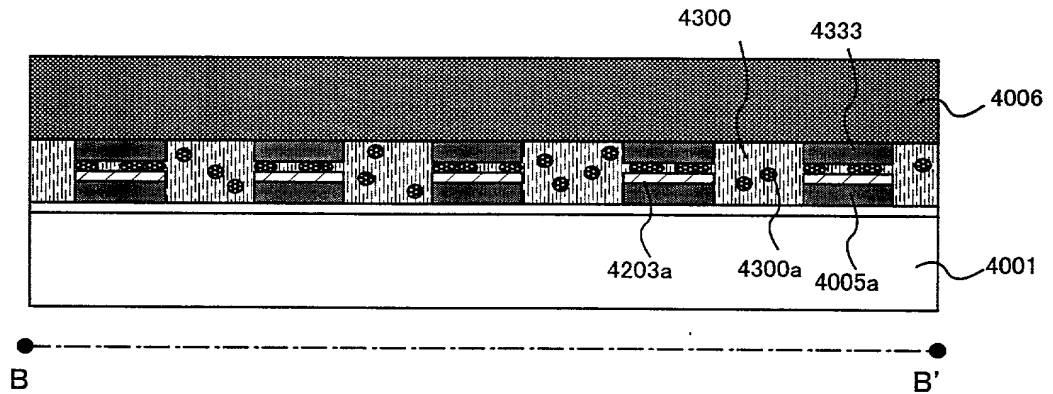


Fig. 19C



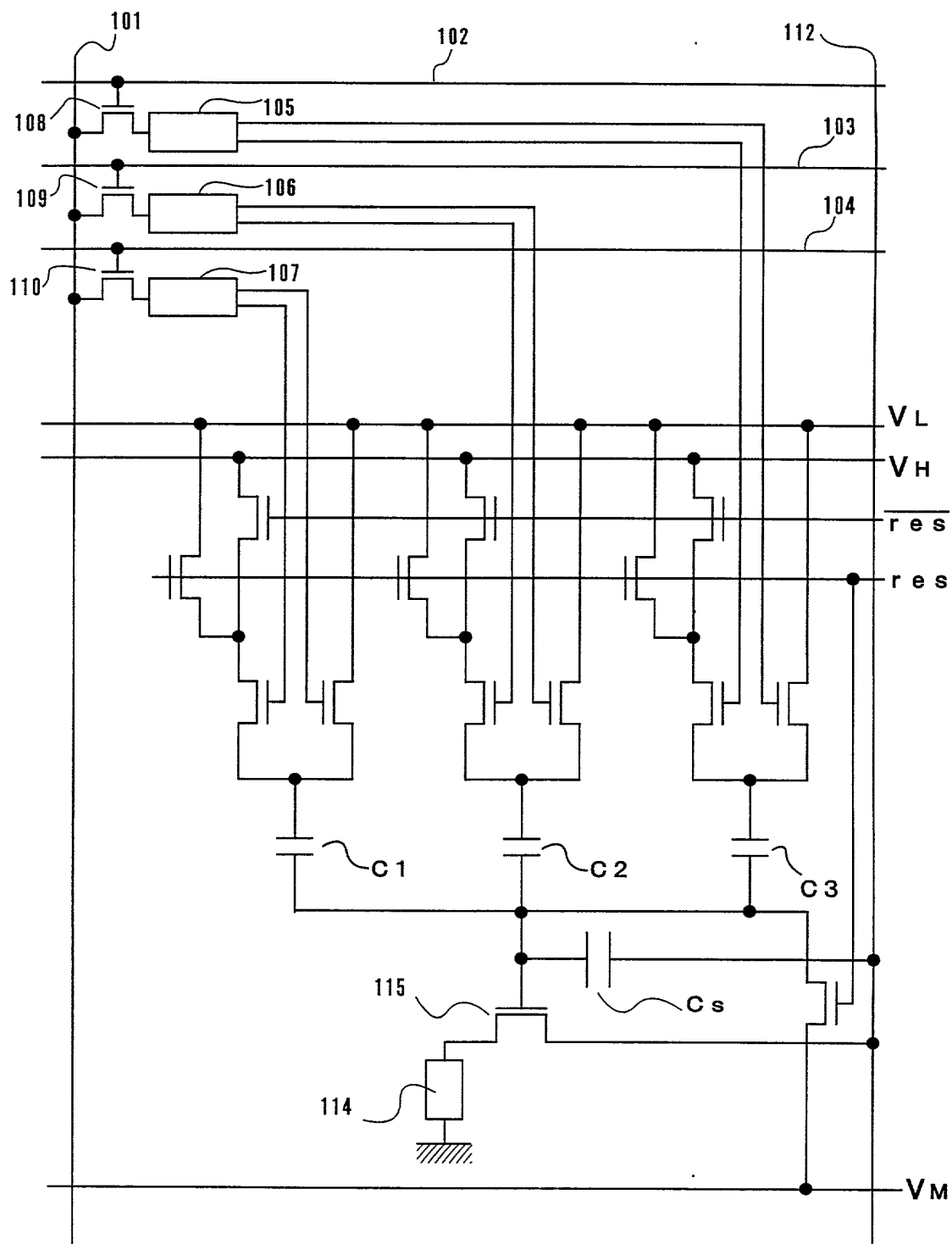


Fig. 21

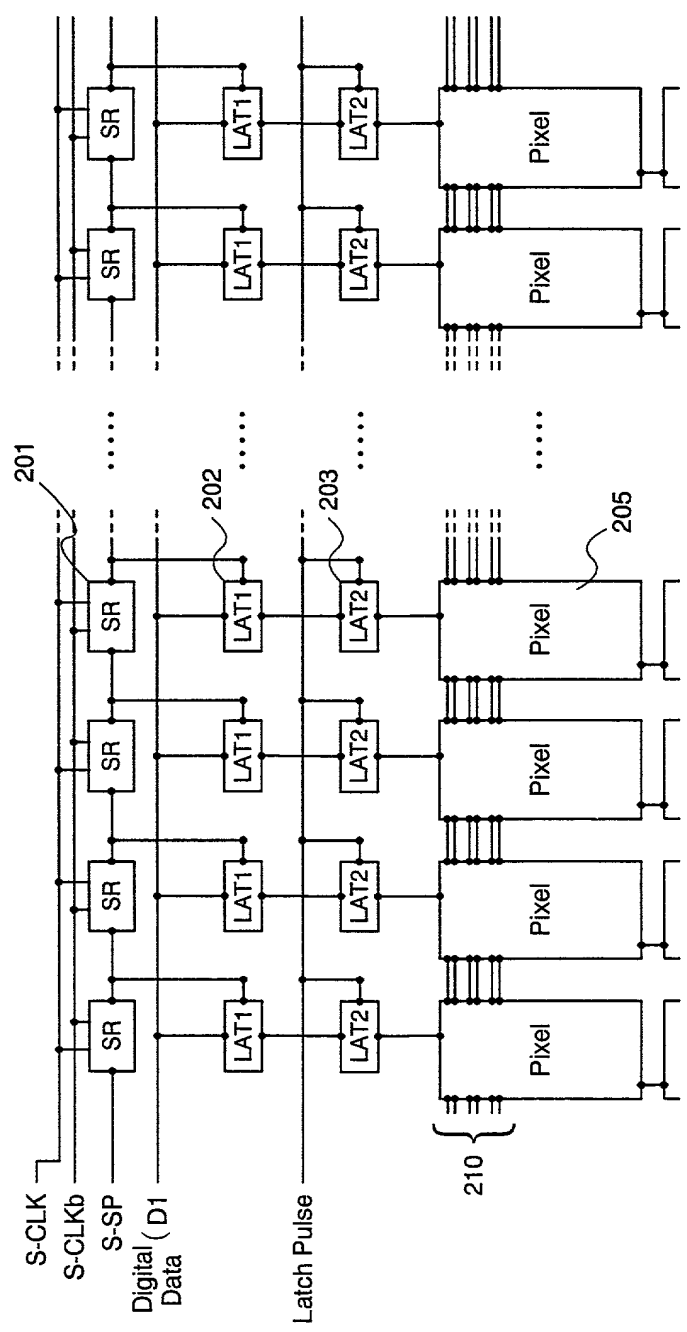


Fig. 22

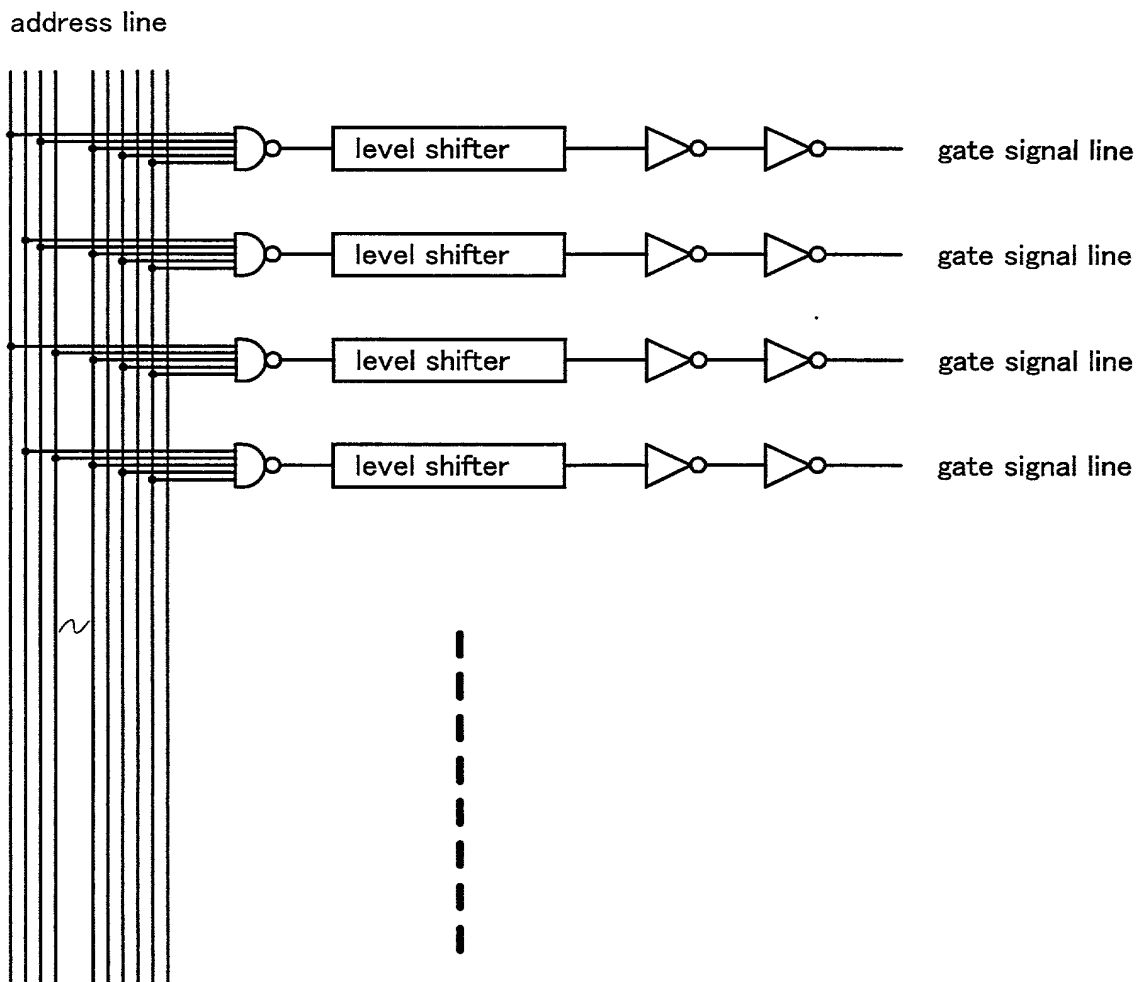


Fig. 23

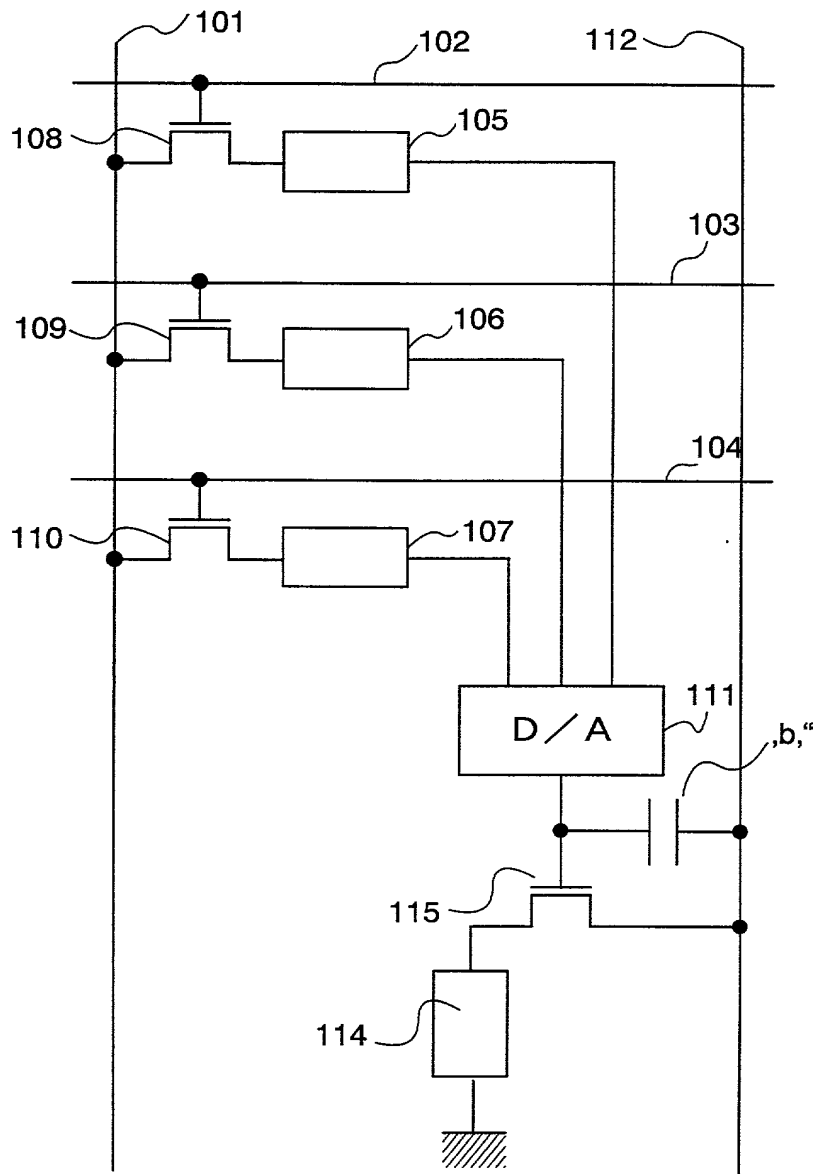


Fig. 24

FIG. 25 is a schematic diagram of a pixel array circuit. The circuit includes a series of shift registers (SR) and latches (LAT1, LAT2) connected to a digital data input (D1, D2, D3) and a latch pulse input. The output of the latches is connected to a bit select input (210) and a series of switches (SW) that control the data flow to the pixel array (205). The pixel array is composed of multiple pixels, each receiving data from the switches and a common data line (201). The circuit is controlled by a series of clock signals (S-CLK, S-CLKb, S-SP) and a latch pulse signal.

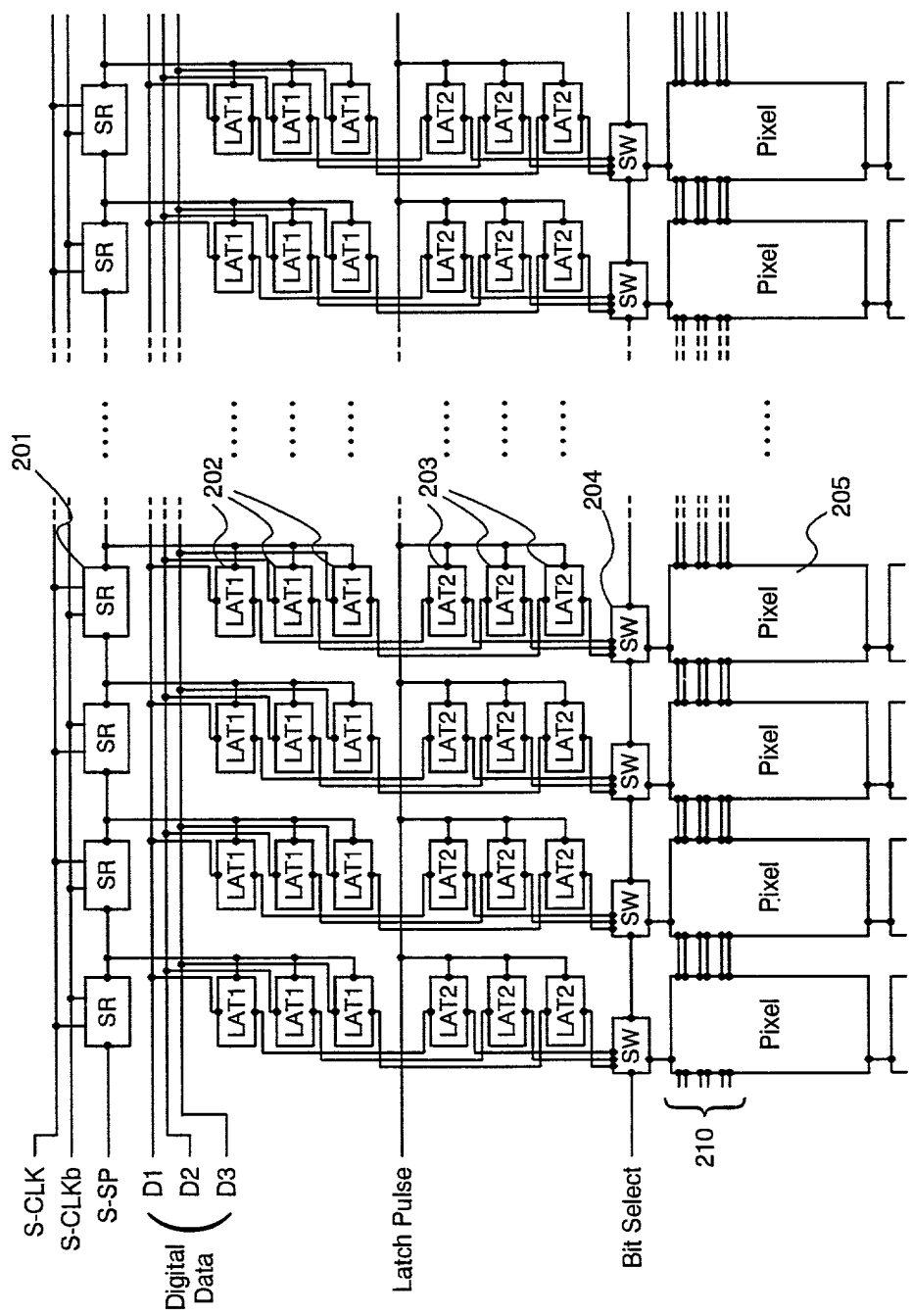


Fig. 25

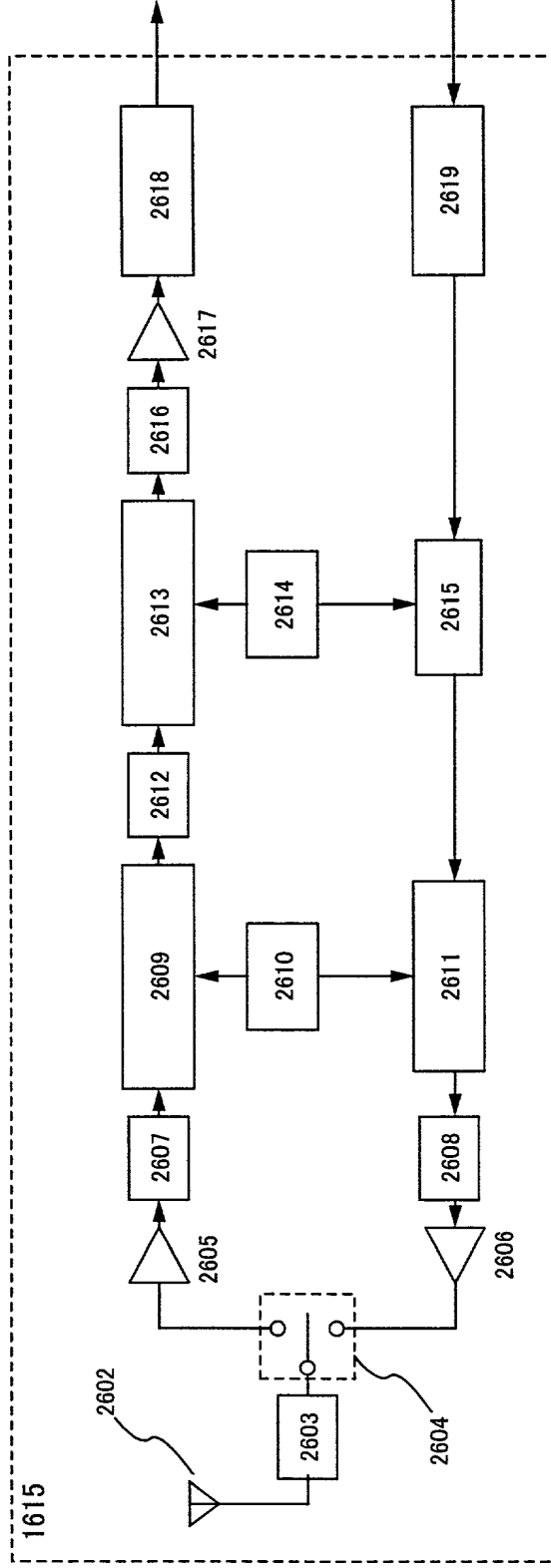


Fig. 26

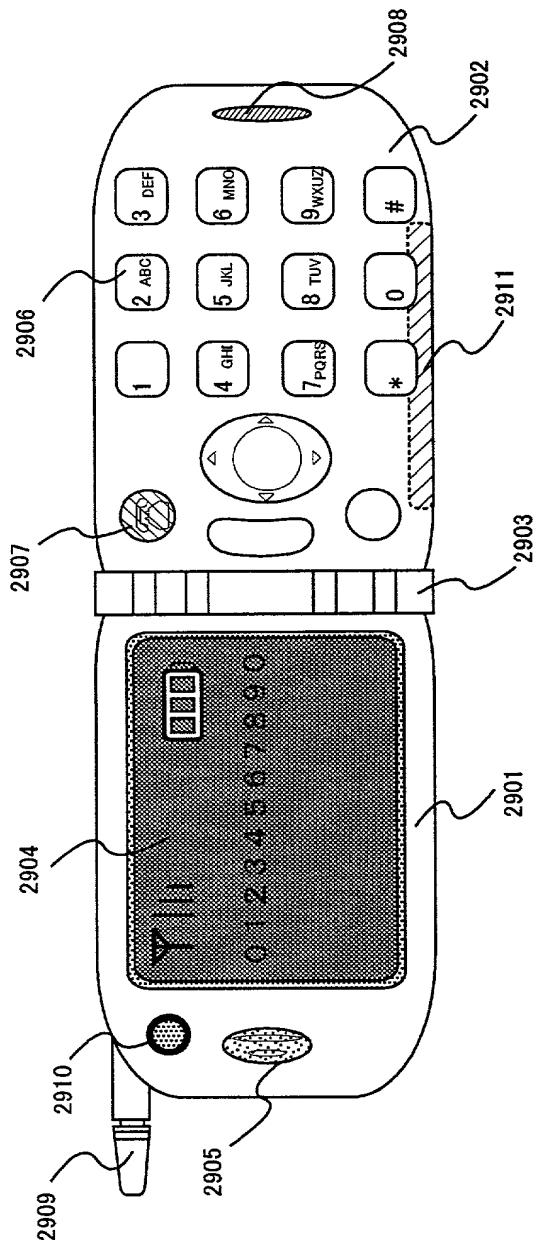


Fig. 27A

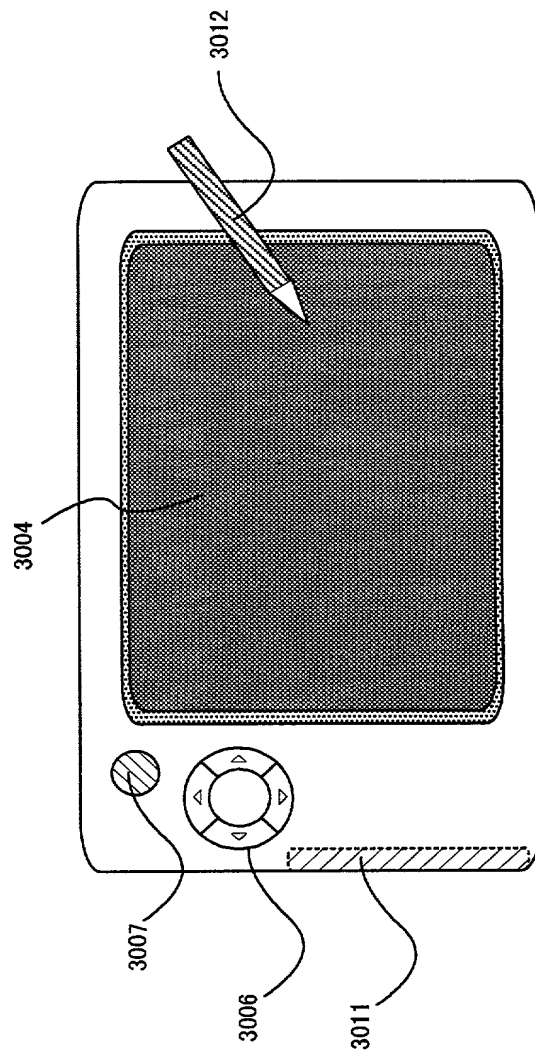


Fig. 27B

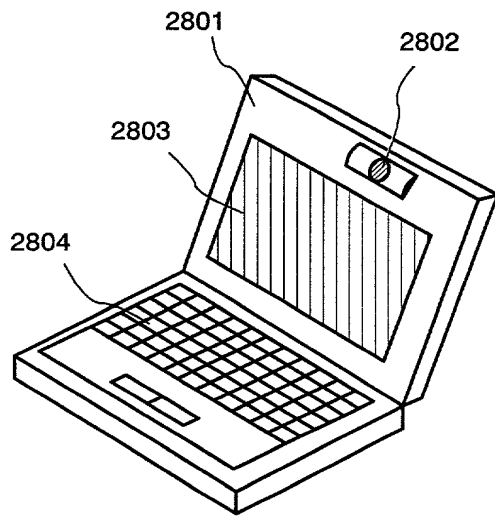


Fig. 28A

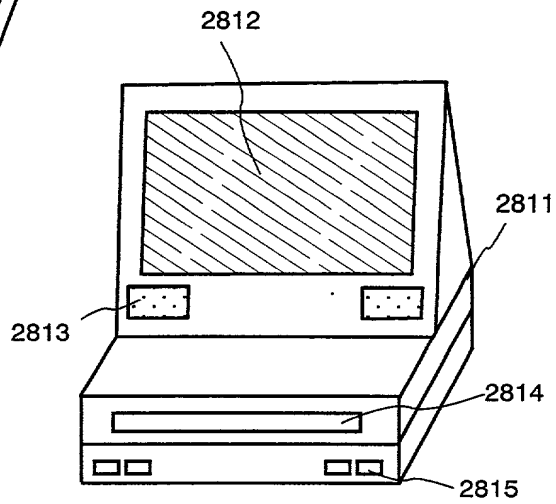


Fig. 28B

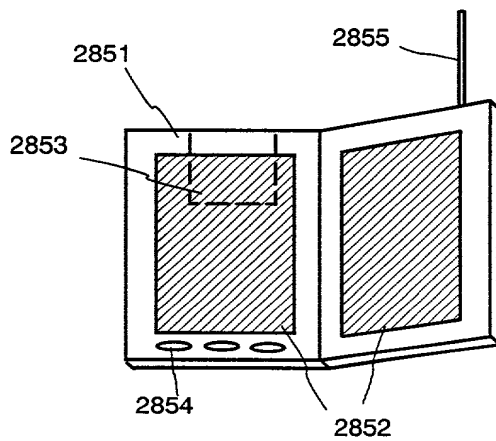


Fig. 28C

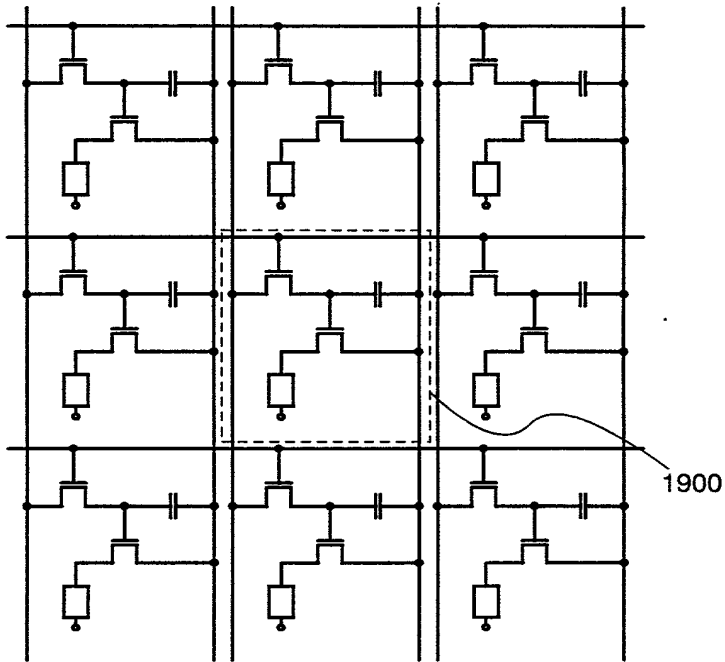


Fig. 29A

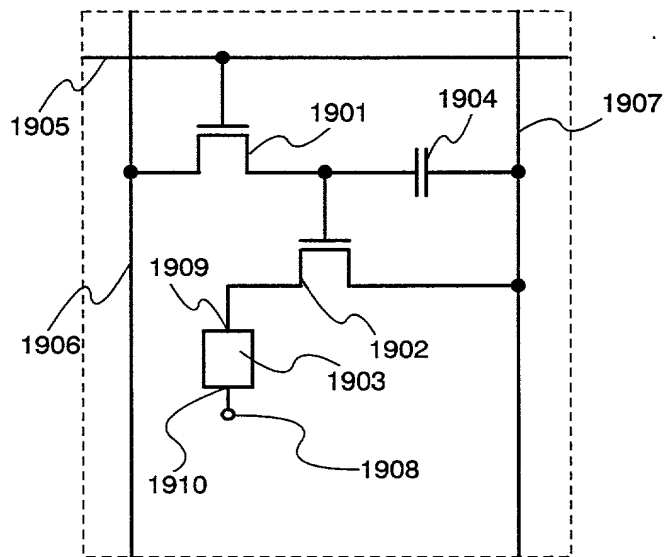


Fig. 29B

Patent Application No. 2016/0100000 A1

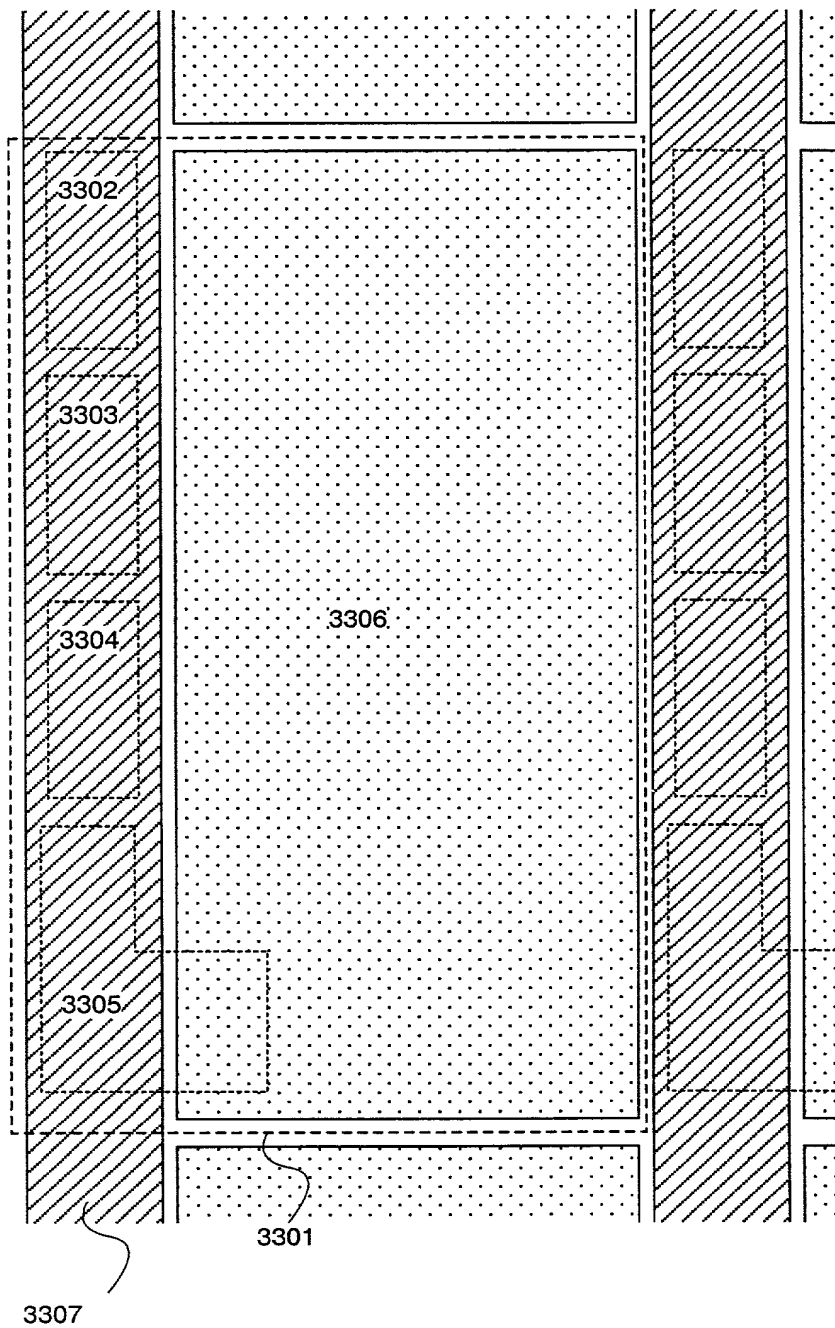


Fig. 30

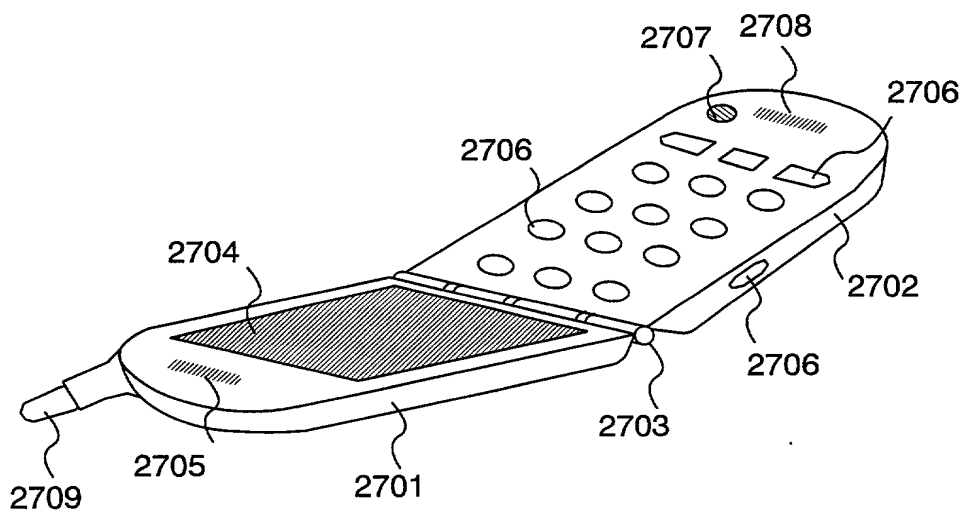


Fig. 31

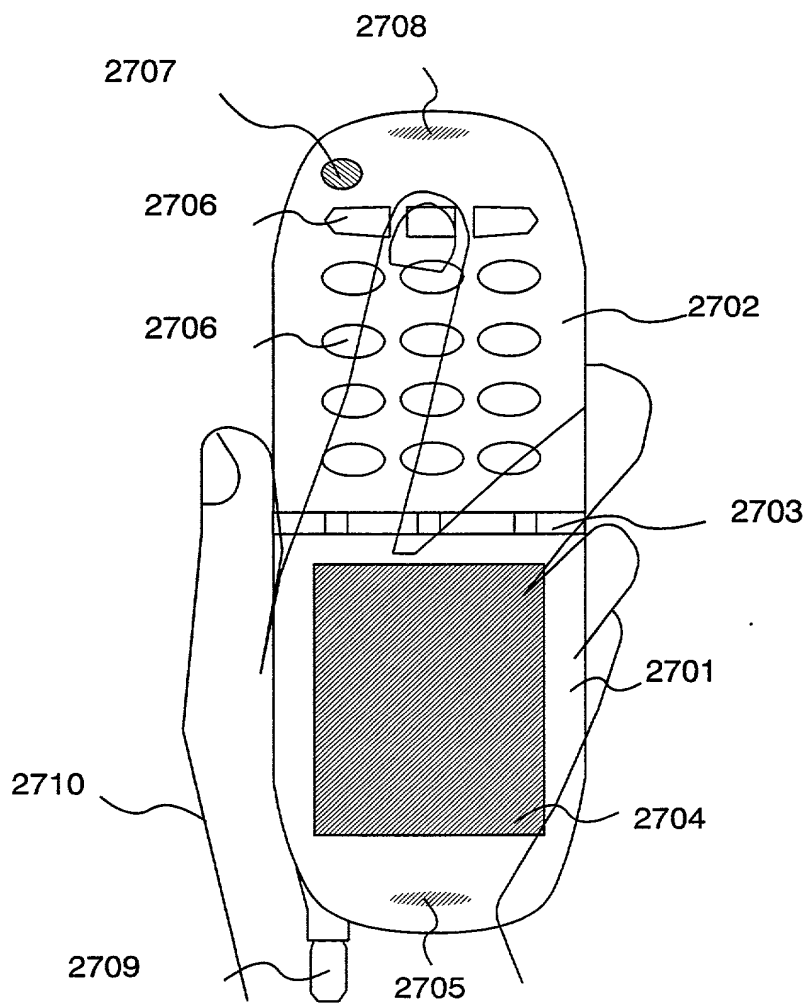


Fig. 32

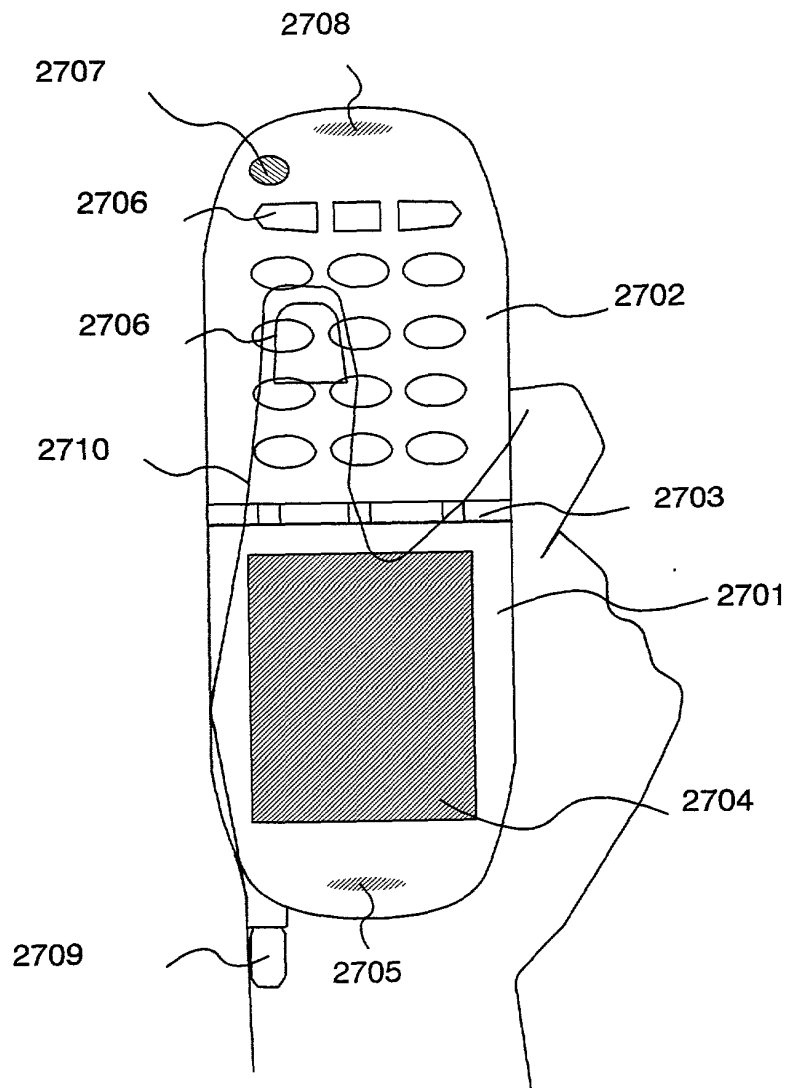


Fig. 33

driving waveform →

optical response waveform →

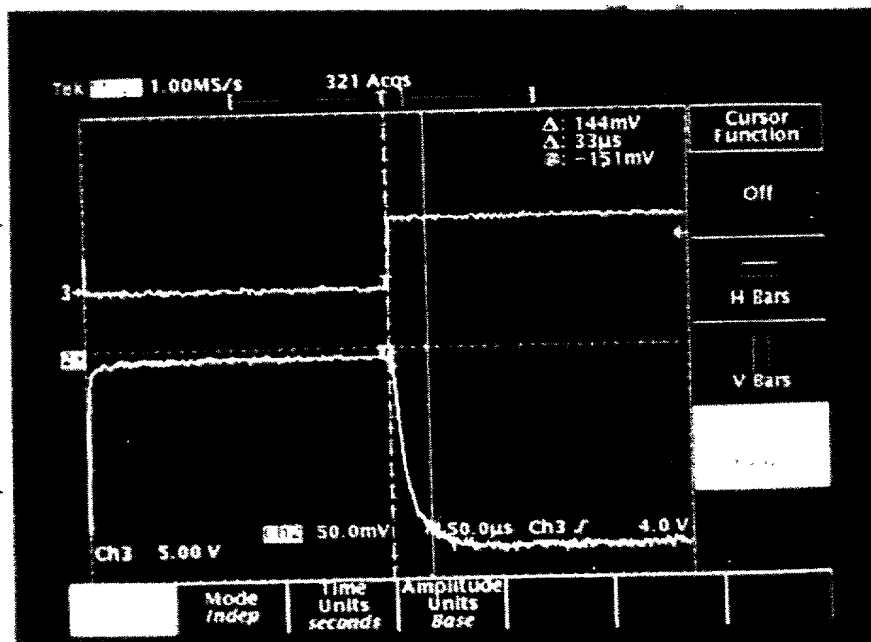


Fig. 34